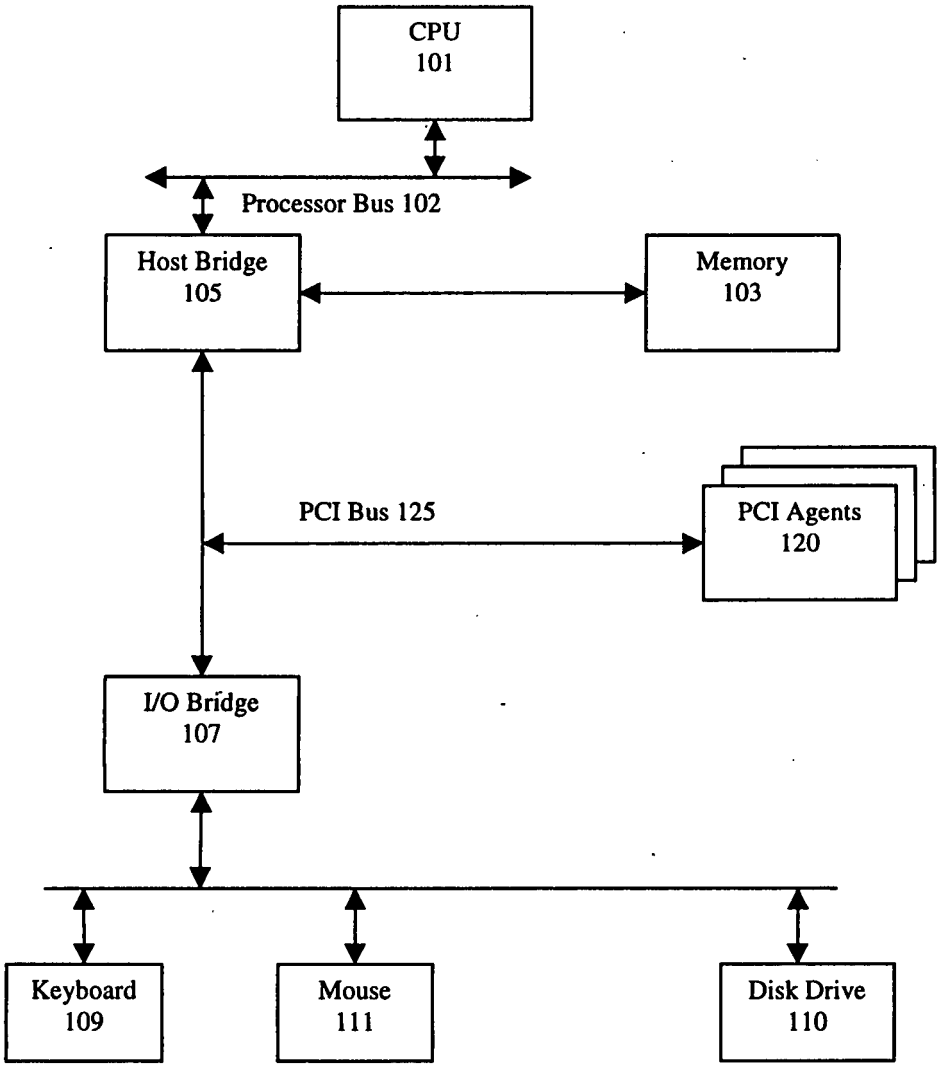

Figure 1A

(Prior Art)

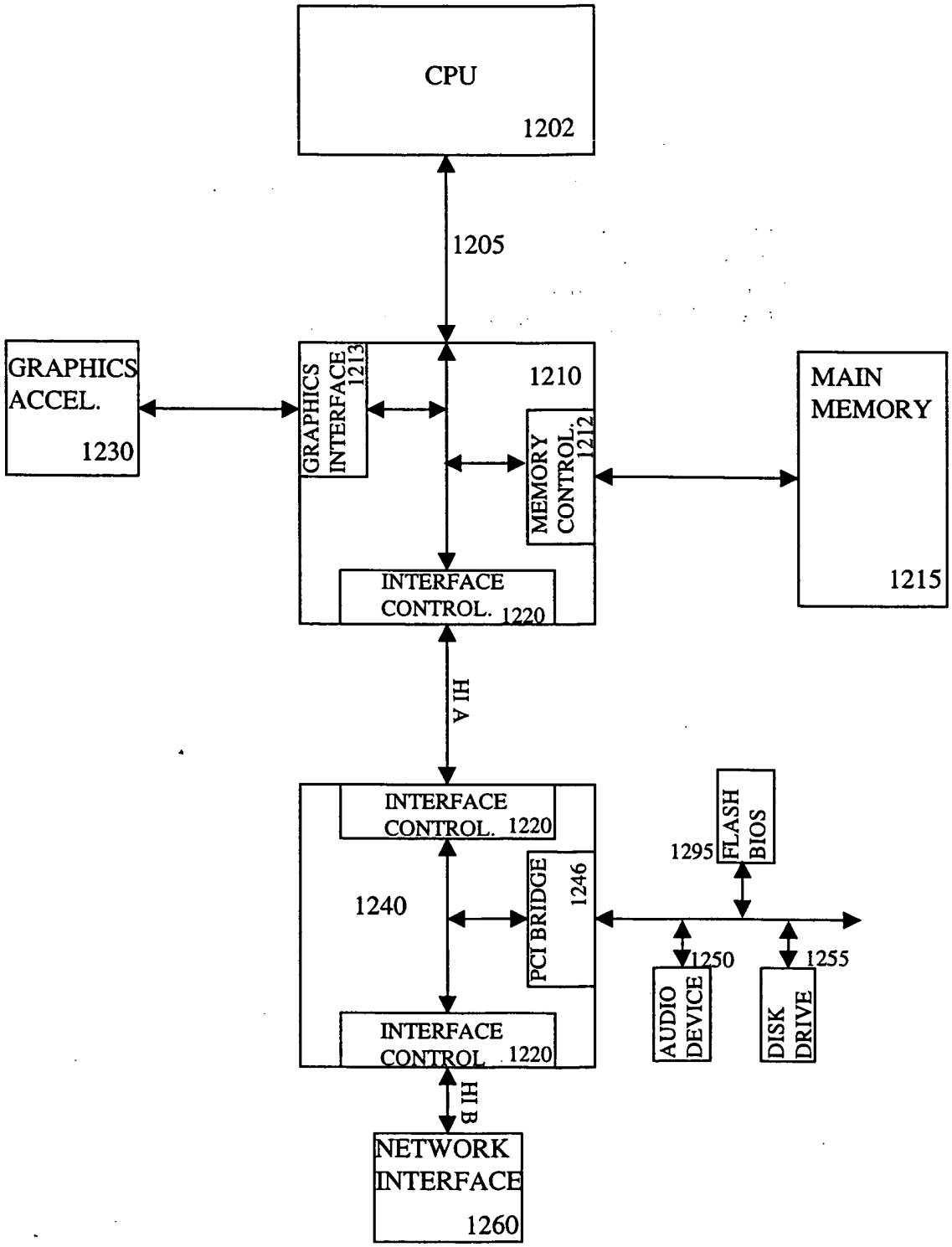
CPU
1202
1205
GRAPHICS ACCEL.
1230
GRAPHICS INTERFACE 1213
1210
MEMORY CONTROL 1212
MAIN MEMORY
1215
INTERFACE CONTROL 1220
HI A
INTERFACE CONTROL 1220
1240
PCI BRIDGE 1246
1295
FLASH BIOS
1250
1255
AUDIO DEVICE
DISK DRIVE
INTERFACE CONTROL 1220
HI B
NETWORK INTERFACE
1260

FIG. 2

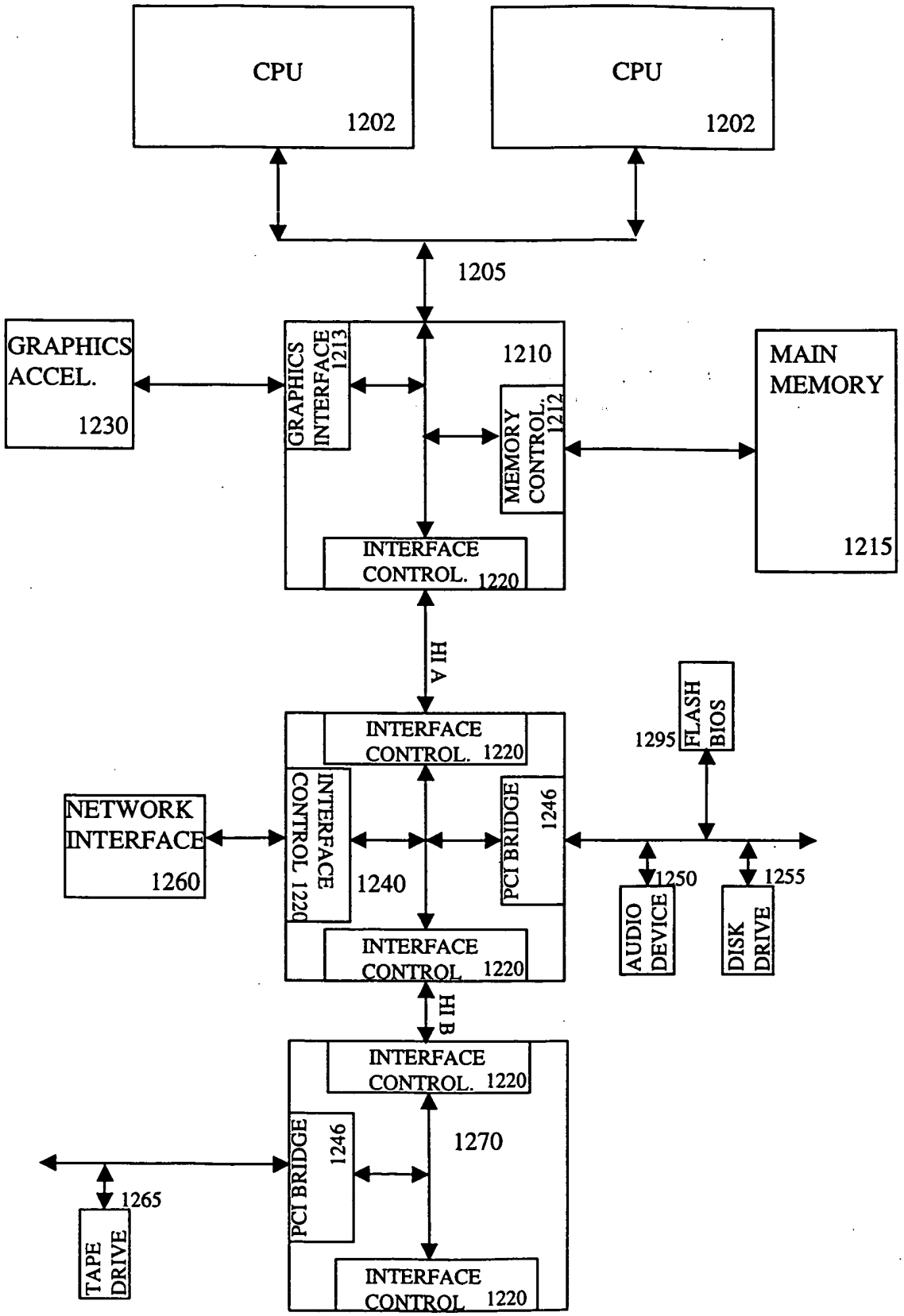
CPU
1202
CPU
1202
1205
GRAPHICS ACCEL.
1230
GRAPHICS INTERFACE 1213
1210
MEMORY CONTROL. 1212
MAIN MEMORY
1215
INTERFACE CONTROL. 1220
HI A
INTERFACE CONTROL. 1220
1295
FLASH BIOS
NETWORK INTERFACE
1260
INTERFACE CONTROL 1224
1240
PCI BRIDGE
1246
1250
1255
AUDIO DEVICE
DISK DRIVE
INTERFACE CONTROL 1220
HI B
INTERFACE CONTROL. 1220
1270
PCI BRIDGE
1246
1265
TAPE DRIVE
INTERFACE CONTROL 1220

FIG. 3

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

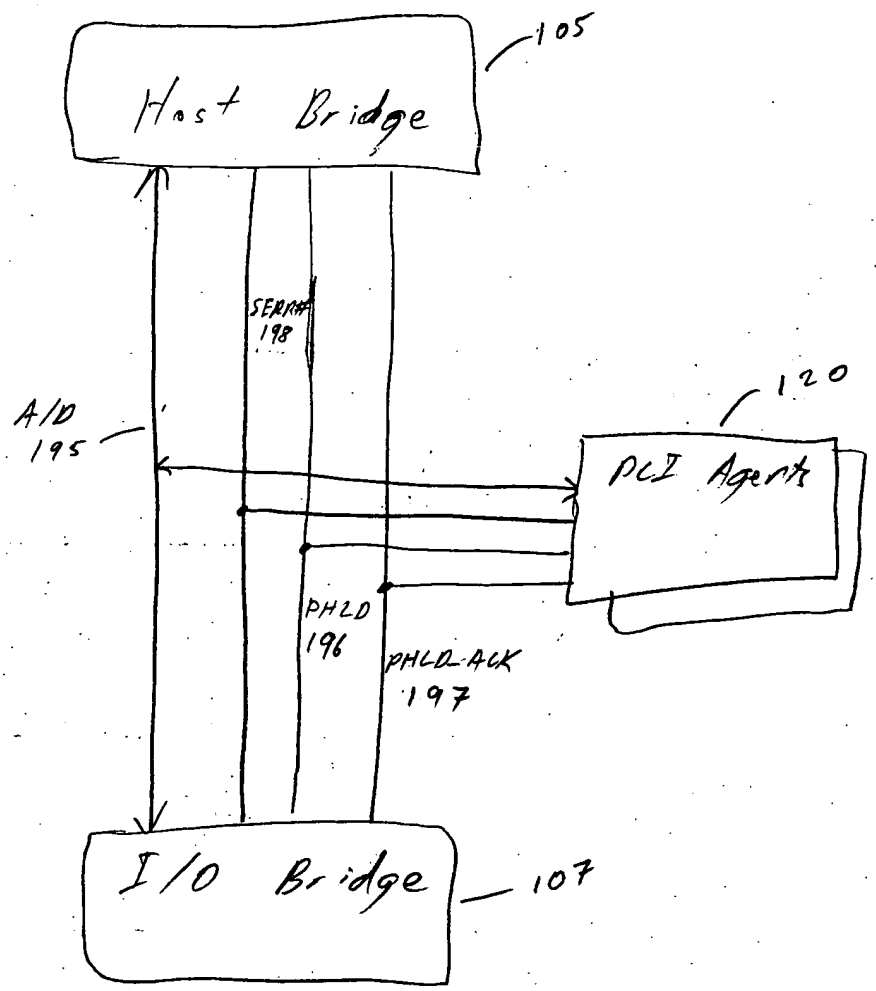

Fig. 1B
(Prior Art)

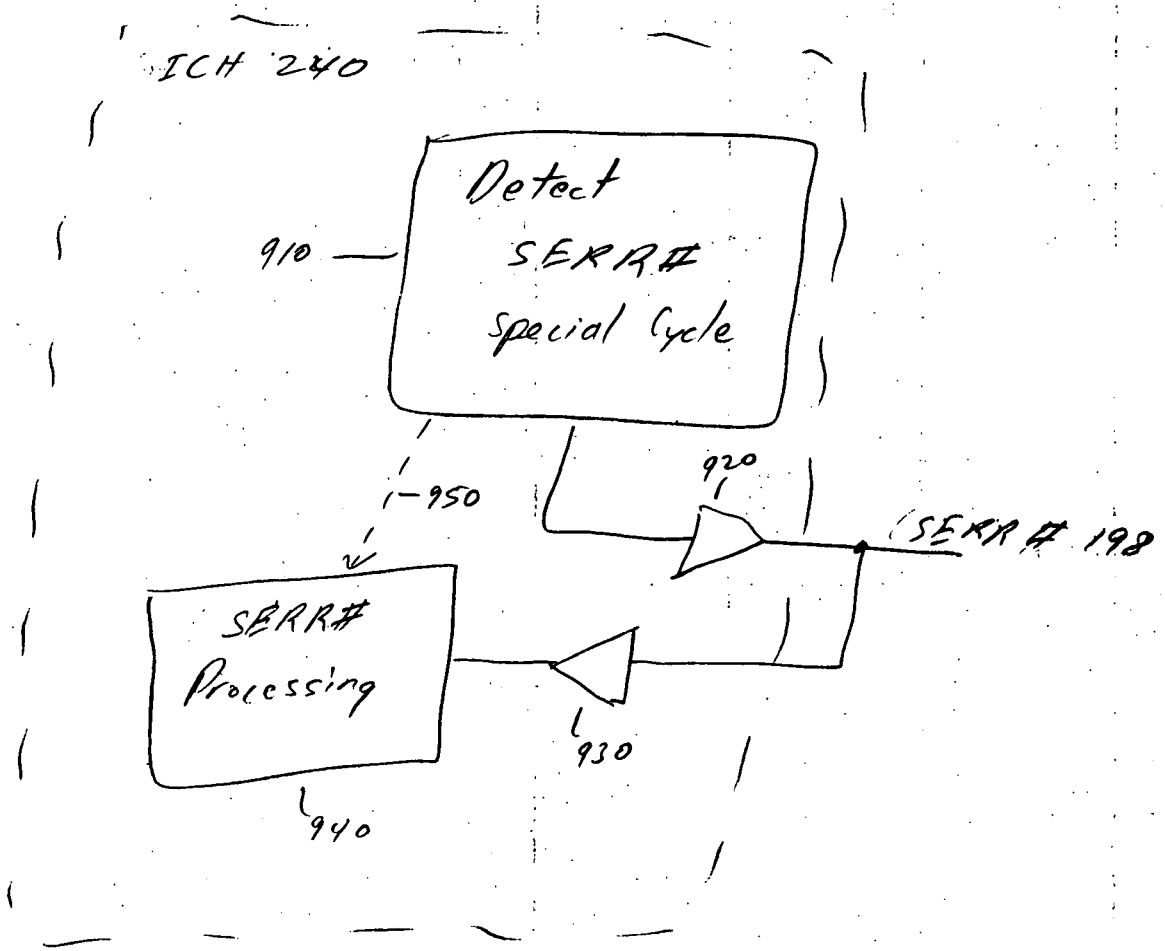

Fig. 4

AMPAD
22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

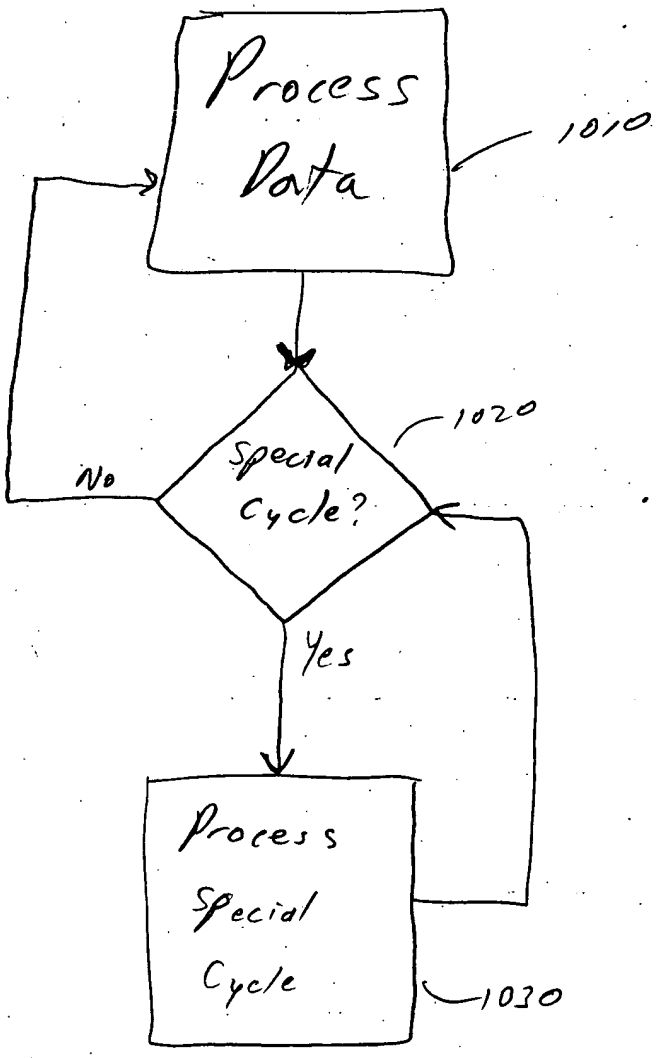

Fig. 5

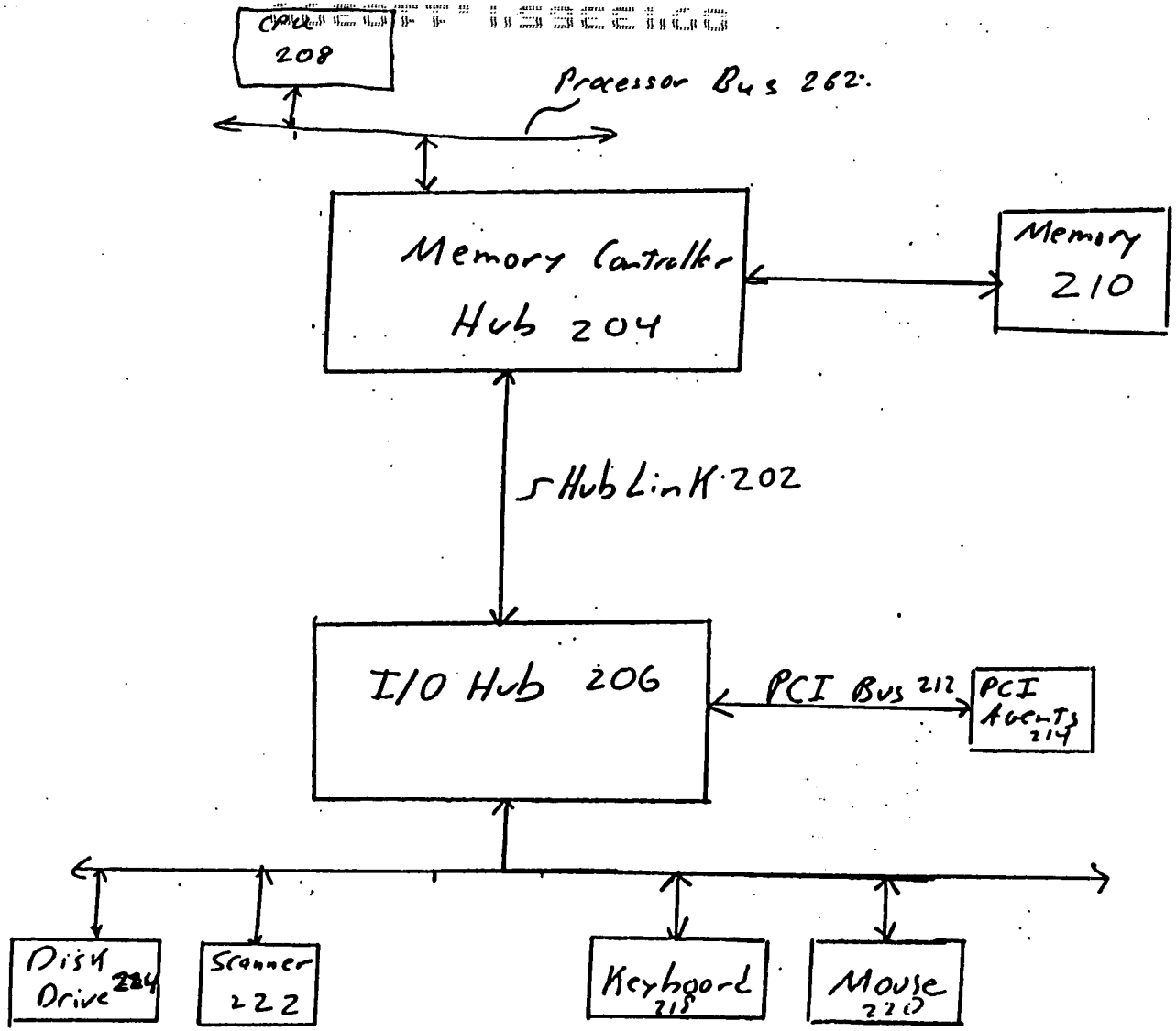
CPU 208
Processor Bus 262
Memory Controller Hub 204
Memory 210
Hub Link 202
I/O Hub 206
PCI Bus 212
PCI Agents 214
Disk Drive 224
Scanner 222
Keyboard 218
Mouse 220

Fig. 6

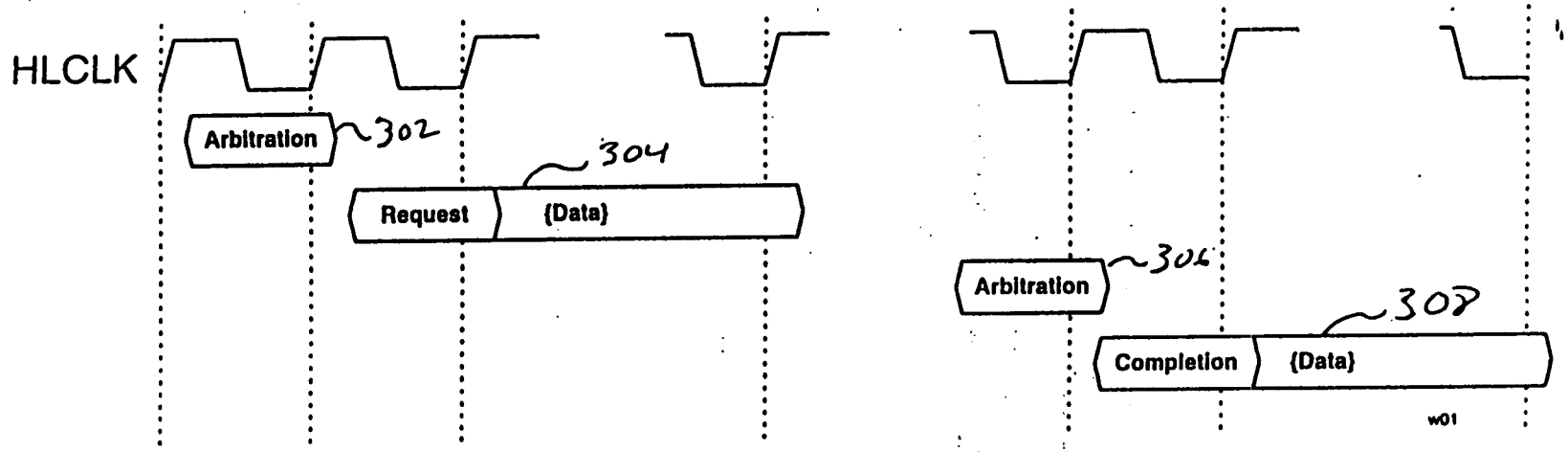
HLCLK
Arbitration
302
304
Request
{Data}
306
Arbitration
307
Completion
{Data}
w01

Fig. 7

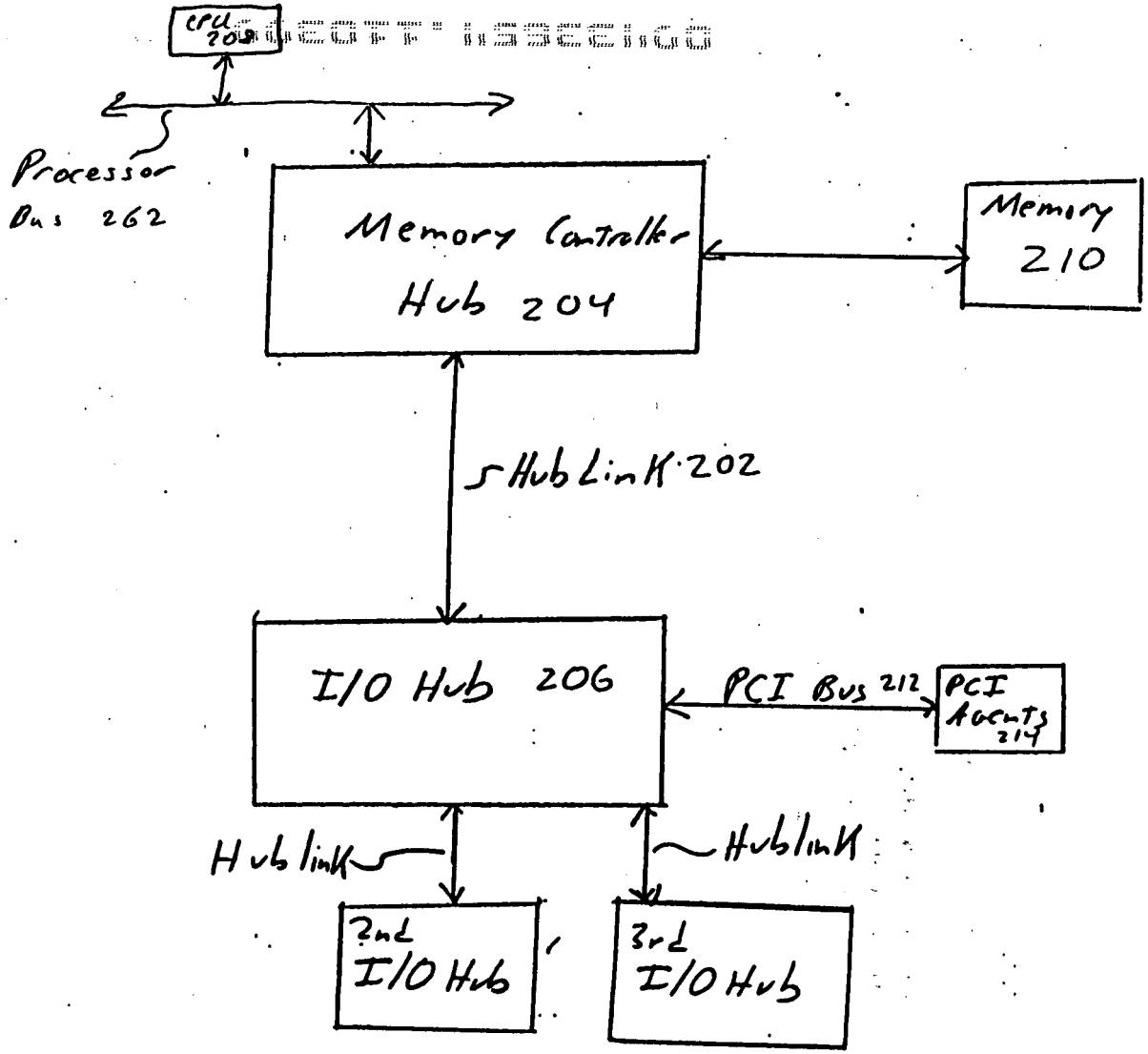
CPU 208
Processor Bus 262
Memory Controller Hub 204
Memory 210
Hub Link 202
I/O Hub 206
PCI Bus 212
PCI Agents 214
Hub link
Hub link
2nd I/O Hub
3rd I/O Hub

Fig. 8

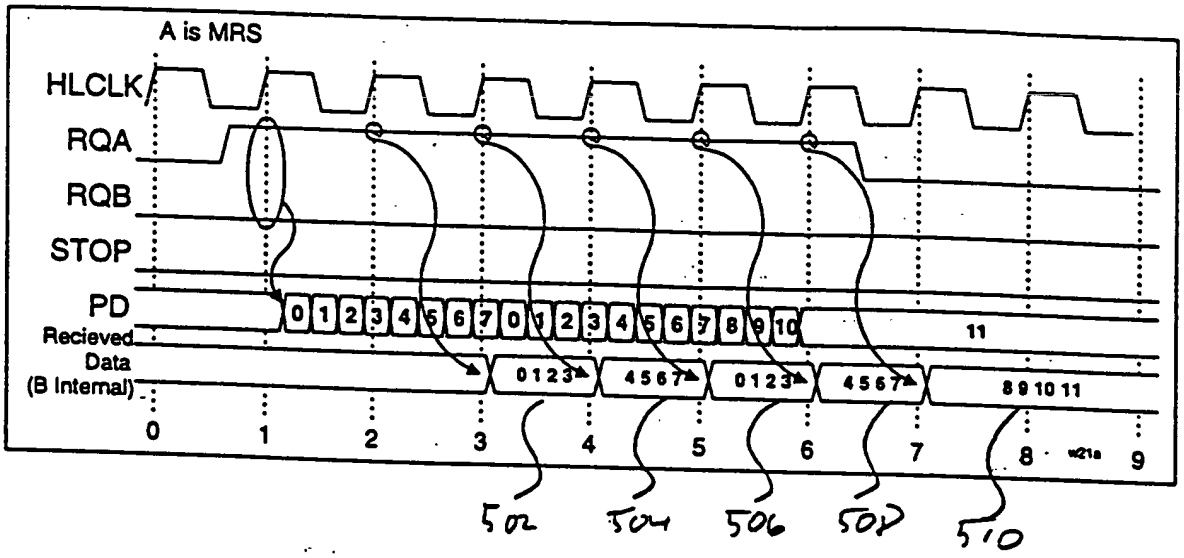
A is MRS
HLCLK
RQA
RQB
STOP
PD
Recieved Data (B Internal)
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 8 9 10
11
0 1 2 3
4 5 6 7
0 1 2 3
4 5 6 7
8 9 10 11
0 1 2 3 4 5 6 7 8 9
502
504
506
508
510

Fig. 9

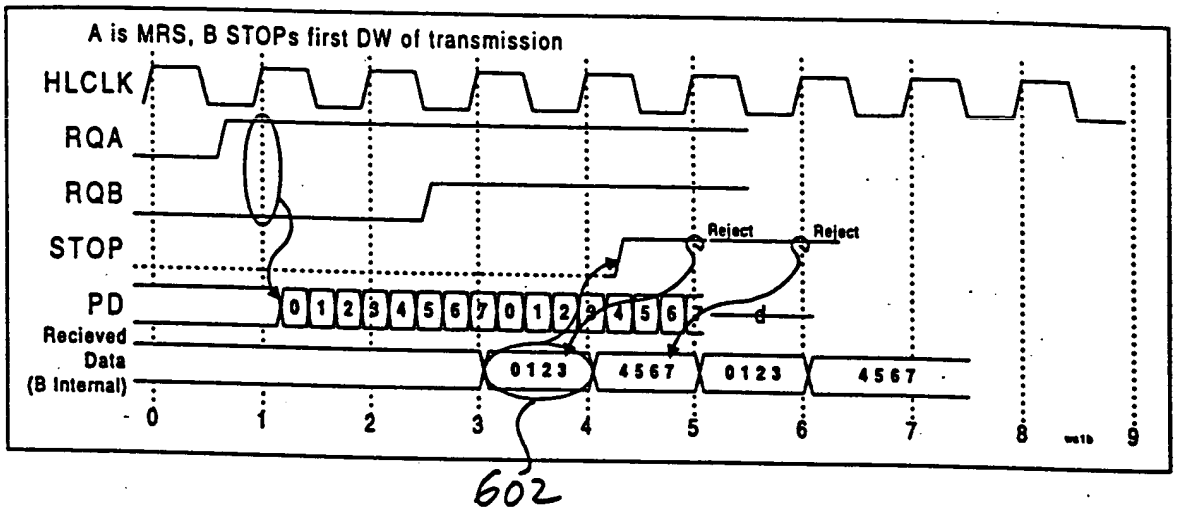
A is MRS, B STOPs first DW of transmission
HLCLK
RQA
RQB
STOP
PD
Recieved Data (B Internal)
Reject
Reject
d
0123
4567
0123
4567
0
1
2
3
4
5
6
7
8
9
602

Fig. 1D

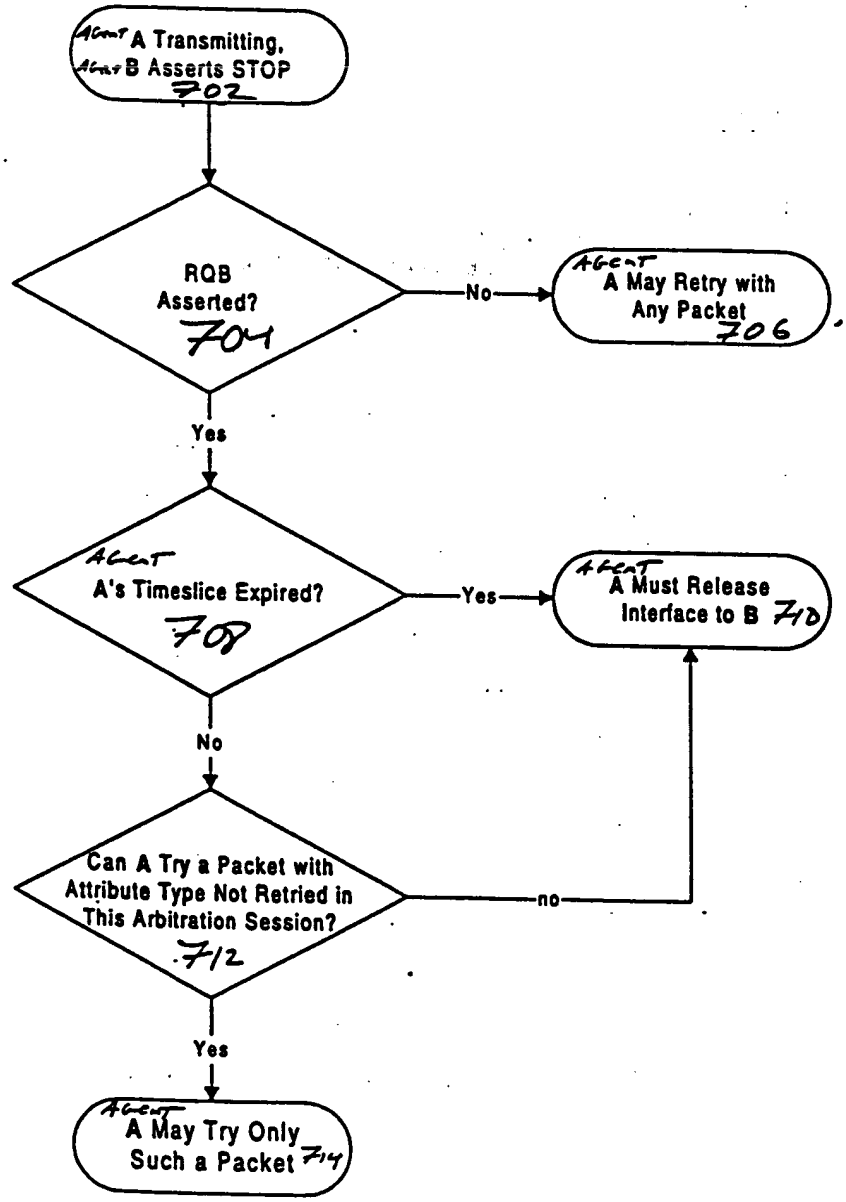
Agent A Transmitting, Agent B Asserts STOP
702
RQB Asserted?
704
No
Agent A May Retry with Any Packet
706
Yes
Agent A's Timeslice Expired?
708
Yes
Agent A Must Release Interface to B
710
No
Can A Try a Packet with Attribute Type Not Retried in This Arbitration Session?
712
no
Yes
Agent A May Try Only Such a Packet
714

Fig. 11

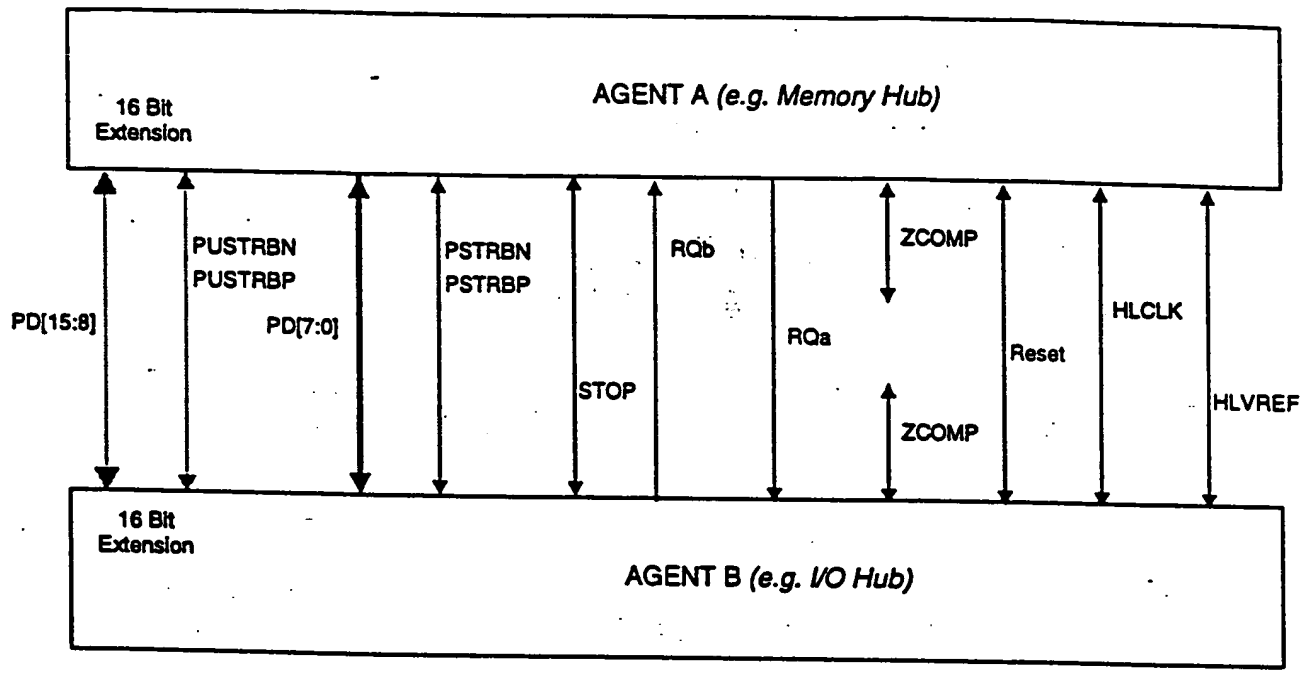
AGENT A (e.g. Memory Hub)
16 Bit Extension
PUSTRBN
PUSTRBP
PD[15:8]
PD[7:0]
PSTRBN
PSTRBP
STOP
RQb
RQa
ZCOMP
ZCOMP
Reset
HLCLK
HLVREF
16 Bit Extension
AGENT B (e.g. I/O Hub)

Fig. 12

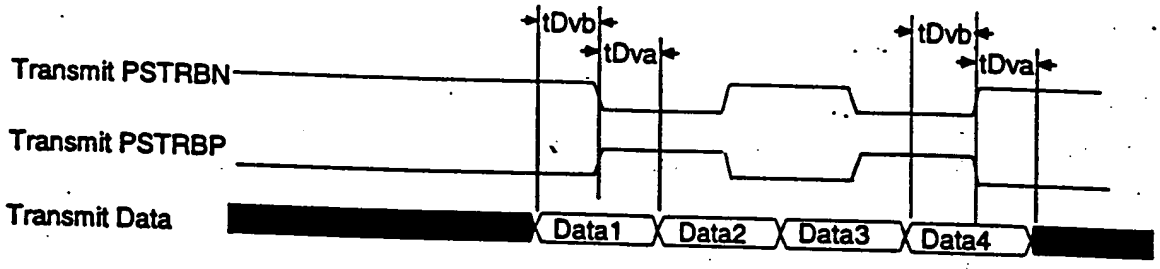
tDvb
tDva
tDvb
tDva
Transmit PSTRBN
Transmit PSTRBP
Transmit Data
Data1
Data2
Data3
Data4

Fig. 13

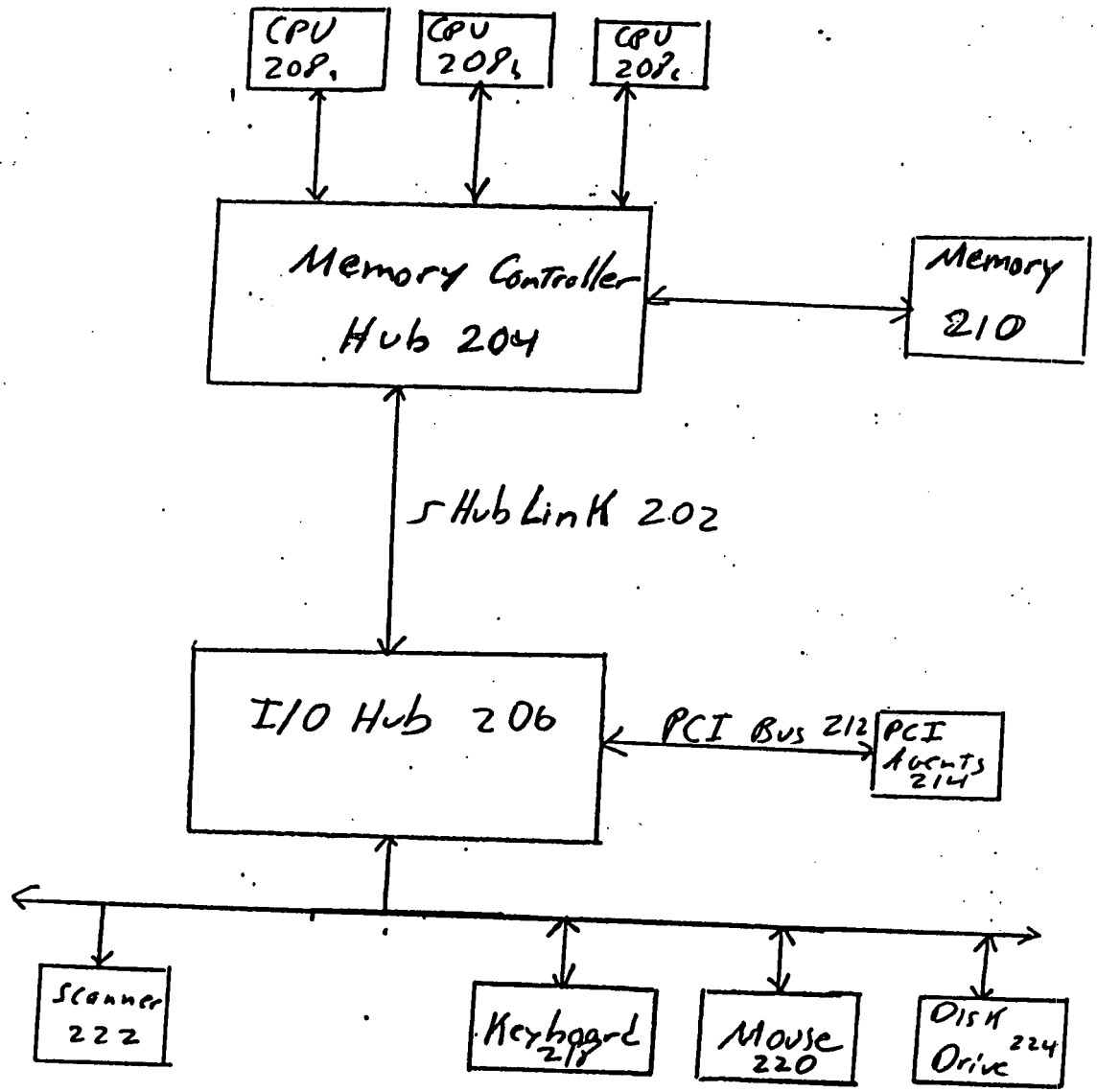
CPU 208a
CPU 208b
CPU 208c
Memory Controller Hub 204
Memory 210
HubLink 202
I/O Hub 206
PCI Bus 212
PCI Agents 214
Scanner 222
Keyboard 218
Mouse 220
Disk Drive 224

Fig. 14